IN THE CLAIMS

Please cancel claims 12-16 without prejudice. These claims will be held for later filing of a divisional application.

Please amend claims 1, 3, 17, 18, and 24 as set forth below.

1. (Amended) A semiconductor device, comprising:

a die attach surface having a first pedestal;

a first semiconductor die having a first surface and an opposed second surface, the first surface being formed with a first cavity [for] mounting the first semiconductor die on the first pedestal and a second smaller cavity within the first cavity underlying a reactive component mounting region defined on the second surface; and

a reactive component disposed on [a] the second surface of the first semiconductor die within [a] the reactive component mounting region overlying the first pedestal.

3. (Amended) A semiconductor device, comprising:

a first semiconductor die having a first surface and an opposed second surface, the first surface being formed with a first cavity and a second smaller cavity within the

first cavity, the second surface having defined thereon a reactive component mounting region overlying the second cavity and an active component mounting region; [and]

a base; and

a first pedestal formed on the base [for engaging] and engaged with the first cavity, where the first pedestal has a recessed region aligned and in communication with the second cavity for forming a dielectric volume underlying the reactive component mounting region.

17. (Amended) An integrated circuit, comprising:

a semiconductor die having a first surface and an opposed second surface, the first surface being formed with a recession, and the second surface being formed with a dielectric platform having a lower surface in the recession and an upper surface defining a reactive component mounting region coplanar with the second surface; [and]

a die attach base having a raised appurtenance [for aligning] aligned with the recession of the semiconductor die and a recessed region in the raised appurtenance; and

[an inductor] a reactive component formed on [a] the second surface of the semiconductor die in the reactive component mounting region to overlie [a] the recessed region of the raised appurtenance.

18. (Amended) A die attach mount, comprising:

a base having a die mounting surface; and

a die attach pedestal formed on the die mounting surface and configured to engage with a first semiconductor die having a cooperating cavity formed in a rear surface, where the die attach pedestal has a recessed region in a surface thereof for forming a dielectric volume[, and] in cooperation with the rear surface of the first semiconductor die [having a first surface formed with a first cavity configured to engage with the die attach pedestal].

24. (Amended) The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar base; and

a frustum of a four-sided pyramid formed from conductive material and having a broad base coupled to a surface of the generally planar base, a height of the frustum being configured to be slightly [less] greater than a depth of [a] the cooperating cavity formed in [a] the rear surface of the first semiconductor die, the recessed region of the frustum [further comprising] includes a small cavity formed on a top surface of the pedestal on regions of the pedestal configured to be placed in proximity to one

or more dielectric platforms formed on the first semiconductor die.

A clean copy of amended claims 1, 3, 17, 18, and 24 is provided below for the Examiner's convenience.

1. A semiconductor device, comprising:

a die attach surface having a first pedestal;

a first semiconductor die having a first surface and an opposed second surface, the first surface being formed with a first cavity mounting the first semiconductor die on the first pedestal and a second smaller cavity within the first cavity underlying a reactive component mounting region defined on the second surface; and

a reactive component disposed on the second surface of the first semiconductor die within the reactive component mounting region overlying the first pedestal.

3. A semiconductor device, comprising:

a first semiconductor die having a first surface and an opposed second surface, the first surface being formed with a first cavity and a second smaller cavity within the first cavity, the second surface having defined thereon a reactive component mounting region overlying the second cavity and an active component mounting region; a base; and

a first pedestal formed on the base and engaged with the first cavity, where the first pedestal has a recessed

region aligned and in communication with the second cavity for forming a dielectric volume underlying the reactive component mounting region.

17. An integrated circuit, comprising:

a semiconductor die having a first surface and an opposed second surface, the first surface being formed with a recession, and the second surface being formed with a dielectric platform having a lower surface in the recession and an upper surface defining a reactive component mounting region coplanar with the second surface;

a die attach base having a raised appurtenance aligned with the recession of the semiconductor die and a recessed region in the raised appurtenance; and

a reactive component formed on the second surface of the semiconductor die in the reactive component mounting region to overlie the recessed region of the raised appurtenance.

18. A die attach mount, comprising:

a base having a die mounting surface; and

a die attach pedestal formed on the die mounting surface and configured to engage with a first semiconductor die having a cooperating recess formed in a rear surface, where the die attach pedestal has a recessed region in a

surface thereof for forming a dielectric volume in cooperation with the rear surface of the first semiconductor die.

24. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar base; and

a frustum of a four-sided pyramid formed from conductive material and having a broad base coupled to a surface of the generally planar base, a height of the frustum being configured to be slightly greater than a depth of the cooperating cavity formed in the rear surface of the first semiconductor die, the recessed region of the frustum includes a small cavity formed on a top surface of the pedestal on regions of the pedestal configured to be placed in proximity to one or more dielectric platforms formed on the first semiconductor die.